REMARKS

Claim 28 is objected to for reasons stated in the Office Action at page 2. The claim is amended such that it is believed that the objection is overcome. Reconsideration of the objection to claim 28 is respectfully requested.

Claims 10-12, 14-17, 23, 25 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki, *et al.* (United States Publication Number 2002/0053943) in view of Sher (United States Patent Number 6,633,196). In view of the amendments to the claims and the following remarks, it is believed that the claims are allowable over the cited references. Accordingly, reconsideration of the rejections is respectfully requested.

With regard to claim 17, claim 17 was previously withdrawn.

With regard to the rejection of independent claim 10, it is submitted that Yamasaki, *et al.* and Sher, taken alone or in combination, fail to teach or suggest a control signal generating circuit for generating a control signal responsive to an input signal related to a number of bits being processed by a semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits, as claimed in amended independent claim 10.

Yamasaki, *et al.* discloses a test mode designating signal TE that activates a driving circuit 2 (see Yamasaki, Figure 1). The test mode designating signal TE is activated/deactivated when a row address strobe signal /RAS, column address strobe signal /CAS, write enable signal /WE, and a specific address signal bit ADD are set to a predetermined combination of states (see Yamasaki, Figures 5A, 5B and page 7, paragraph [0092]). However, the claimed invention is different than Yamasaki, *et al.*, since, in the present invention, a control signal is activated when an input signal indicates that a number of data bits being processed by a semiconductor device is

more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits, as claimed. On the other hand, there is no teaching or suggestion in Yamasaki, *et al.* of the row address strobe signal /RAS, column address strobe signal /CAS, write enable signal /WE, or specific address signal bit ADD being an input signal related to a number of bits processed by a semiconductor device. Nor is there any teaching or suggestion in Yamasaki, *et al.* of the test mode designating signal TE being activated when an input signal indicates that a number of data bits being processed by a semiconductor device is more than a predetermined number of bits, and the test mode designating signal TE being inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits. It therefore follows that Yamasaki, *et al.* fails to teach or suggest Applicants' claimed control signal generating circuit.

Sher discloses a programmable circuit, wherein a control voltage Vselect is applied to NMOS transistors 38, 40 (see Sher, Figure 3A) and transistors 46, 48, 50, 52 (see Sher, Figure 3B). However, there is no teaching or suggestion of the control voltage Vselect being activated when an input signal indicates that a number of data bits being processed by a semiconductor device is more than a predetermined number of bits, and the control voltage Vselect being inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits, as claimed. It therefore follows that Sher likewise fails to teach or suggest Applicants' claimed control signal generating circuit.

In addition, it is submitted that Yamasaki, *et al.* and Sher, taken alone or in combination, fail to teach or suggest a switching circuit coupled to an output of a comparing circuit for transmitting a comparing signal as a driving signal when the control signal is inactivated, as claimed in amended independent claim 10. Specifically, neither Yamasaki, *et al.* nor Sher teaches a control signal, as claimed, for reasons described herein. Further, Yamasaki, *et al.* fails to teach a switching circuit coupled to an output of a comparing circuit. The drive

transistor DR of Yamasaki, *et al.* is not Applicants' claimed switching circuit because there is no teaching or suggestion in Yamasaki, *et al.* of drive transistor DR transmitting a comparing signal as a driving signal when the control signal is inactivated, as claimed in amended independent claim 10. Instead, the internal voltage down converter VDC of Yamasaki, *et al.*, which includes a comparator CMP and drive transistor DR, is analogous to the Applicant Admitted Prior Art (AAPA), as illustrated in Figure 1 of Applicants' drawings.

Sher likewise fails to teach a switching circuit coupled to an output of a comparing circuit, as claimed in claim 10.

With regard to the rejection of claim 23, it is submitted that Yamasaki, *et al.* and Sher, taken alone or in combination, fail to teach or suggest a control signal generating circuit for generating a control signal responsive to an input signal related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits, as claimed in independent claim 23, for at least reasons similar to those described above.

In addition, it is submitted that Yamasaki, *et al.* and Sher, taken alone or in combination, fail to teach or suggest an internal voltage generating circuit coupled to a control signal generating circuit for receiving a control signal and comparing a reference voltage to an internal voltage to make the internal voltage have the reference voltage level in response to a driving signal when the control signal is inactivated, and to make the internal voltage have an external power voltage level when the control signal is activated, for at least reasons similar to those described above.

Accordingly, it is submitted that Yamasaki, *et al.* and Sher, taken alone or in combination, fail to teach or suggest the invention set forth in the claims. Since the combination of Yamasaki, *et al.* and Sher fails to teach or suggest the invention set forth in the claims, the

claims are believed to be allowable over the cited references. Accordingly, reconsideration and removal of the rejection of claims 10-12, 14-17, 23, 25, and 27-29 under 35 U.S.C. 103(a) based on the combination of Yamasaki, *et al.* and Sher are respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

Date: 11/6/06

Mills & Onello, LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900
Facsimile: (617) 742-7774
J:\SAM\0529\amendmentd.doc

Steven M. Mills
Registration Number 36,610
Attorney for Applicants